AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A memory system comprising:

a multi-bank memory having a first memory bank and a second memory bank;

a muxing circuit coupled to the multi-bank memory;

a first memory access device coupled to muxing circuit; and

a second memory access device coupled to the muxing circuit;

wherein the muxing circuit is configurable to couple the first access device to the first memory bank to read and write non-interleaved data and to discretely and simultaneously couple the second access device to the second memory bank to read and write non-interleaved data ~~simultaneously~~, and the muxing circuit is configurable to couple the second access device to the first memory bank to read and write non-interleaved data and to discretely and simultaneously couple the first access device to the second memory bank to read and write non-interleaved data ~~simultaneously~~.

2. (Original) The memory system of Claim 1, wherein the multi-bank memory comprises a third memory bank and wherein the muxing circuit is configurable to couple the first access device to the third memory bank and the muxing circuit is configurable to couple the second access device to the third memory bank.

3. (Original) The memory system of Claim 1, further comprising a third memory access device coupled to the muxing circuit and wherein the muxing circuit is configurable to couple the third access device to the first memory bank and the second memory bank.

4. (Canceled)

5. (Canceled)

6. (Original) The memory system of Claim 1, wherein the first memory bank is larger than the second memory bank.

7. (Original) The memory system of Claim 1, wherein the first memory bank operates at a first frequency and the second memory bank operates at a second frequency, wherein the first frequency is greater than the second frequency.

8. (Original) The memory system of Claim 1, wherein the first memory bank is of a first memory type and the second memory bank is of: a second memory type.

9. (Original) The memory system of Claim 8, wherein the first memory type is DRAM and the second memory type is SRAM.

10. (Original) The memory system of Claim 1, wherein the first memory access device is a CPU.

11. (Original) The memory system of Claim 1, wherein the second memory access device is a DMA controller.

12. (Withdrawn) A method of processing a plurality of data sets on a memory system having a first memory bank and a second memory bank; the method comprising:

storing a first data set in the first memory bank; processing the first data set;

storing a second data set in the second memory bank; processing the second data set; and

storing a third data set in the first memory bank.

13. (Withdrawn) The method of Claim 12 wherein the processing the first data set and the storing a second data set in the second memory bank occurs simultaneously.

14. (Withdrawn) The method of Claim 12, further comprising processing the third data set in the first memory bank.

15. (Withdrawn) The method of Claim 12, further comprising requesting use of the first memory bank for a first memory access device before the storing a first data set in the first memory bank.

16. (Withdrawn) The method of Claim 15, further comprising requesting use of the first memory bank for a second memory access device before the processing the first data set.

17. (Withdrawn) The method of Claim 16, further comprising stalling the second memory access device until after the first data set is stored in the first memory bank.

18. (Withdrawn) The method of Claim 17, further comprising requesting the first memory bank for the first memory access device before storing a third data set in the first memory bank.

19. (Withdrawn) The method of Claim 18, further comprising stalling the first memory access device until after the first data set is processed.

20. (Withdrawn) The method of Claim 12, wherein the first data set, the second data set, and the third data set are stored by a first memory access device.

21. (Withdrawn) The method of Claim 20, wherein the first data set and the second data set are processed by a second memory access device.

22. (Withdrawn) The method of Claim 21, wherein the first memory access device is a DMA controller and the second memory access device is a CPU.

23. (Withdrawn) The method of Claim 12, wherein the memory system has a third memory bank and further comprising storing a fourth data set in the third memory bank.

24. (Withdrawn) The method of Claim 12, wherein the first data set is stored by a first memory access device.

25. (Withdrawn) The method of Claim 24, wherein the first data set is processed by a second memory access device.

26. (Withdrawn) The method of Claim 25, wherein second data set is stored by a third memory access device.

27. (Withdrawn) A memory system for processing a plurality of data sets comprising:

a first memory bank;

a second memory bank;

means for storing a first data set in the first memory bank;

means for processing the first data set;

means for storing a second data set in the second memory bank;

means for processing the second data set; and

means for storing a third data set in the first memory bank.

28. (Withdrawn) The memory system of Claim 27, further means for comprising processing the third data set in the first memory bank.

29. (Withdrawn) The memory system of Claim 27, further comprising means for requesting use of the first memory bank for a first memory access device.

30. (Withdrawn) The memory system of Claim 29, further comprising means for requesting use of the first memory bank for a second memory access device.

31. (Withdrawn) The memory system of Claim 30, further comprising means for stalling the second memory access device.

32. (Withdrawn) The memory system of Claim 27, wherein the first data set, the second data set, and the third data set are stored by a first memory access device.

33. (Withdrawn) The memory system of Claim 32, wherein the first data set and the second data set are processed by a second memory access device.

34. (Withdrawn) The memory system of Claim 33, wherein the first memory access device is a DMA controller and the second memory access device is a CPU.